Making the Move from 28nm to 16nm FinFET - Easy as POP

ARM Inc



ABSTRACT

There are many ARM based partners that want to move from manufacturing in the traditional CMOS process technology to the exciting FinFET process, but may be unsure of the challenges faced when moving to a FinFET process technology. While the TSMC 16FFC process is lower cost FinFET process that targets a wide range of applications. The physical design group at ARM have developed implementation solutions in both TSMC 28HPC+ as well as TSMC 16FFC, and have uncovered findings that will optimize and accelerate the implementation of ARM based SoC designs. Using ARM's latest processor, Cortex-A73 as a case study, this paper will summarize deep technical findings and learnings from various implementation trials. It will cover process differences, power grid creation challenges, floor planning differences (due to fin pitch requirements), key enhancements in clock tree synthesis and revised sign off criteria.

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Physical design group

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Agenda

- Why FinFet?
 - How can 16FFC help?
 - Differences in two technology (planner versus finFET)
- Implementation results using ARM's latest core
 - Cortex-A73 using TSMC 28HPC+ and TSMC 16FFC process
- Key differences between two processes for floor planning, power planning and clock tree synthesis
 - How we make physical design easier!
- PPA (Power Performance and Area) differences using two processes

The new threshold for market leadership

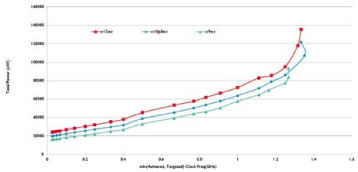


Hisilicon
MediaTek
Spectrum…
…have announced plans to move to 16nm form 28nm

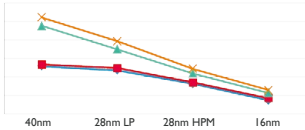
Why FinFET ? FinFET Power, Performance and Area

- Comparisons on process- or IP-level not very useful
 - Don't compare gates
 - Don't compare bitcells
 - Compare at SoC-level or critical block-level
- Much higher performance of finFETs allows new optimization approaches

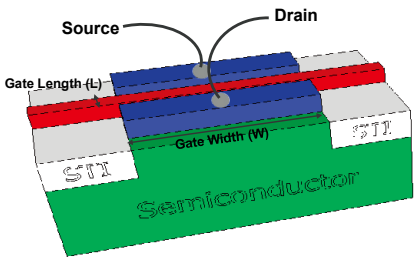
Standard cell Performance vs Leakage on Cortex-Ax



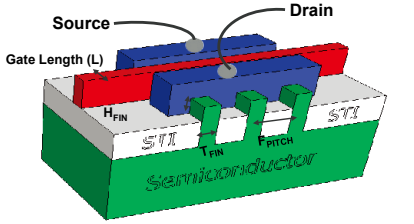
Compiler Memory Access Time



What is a FinFET?



Traditional Bulk

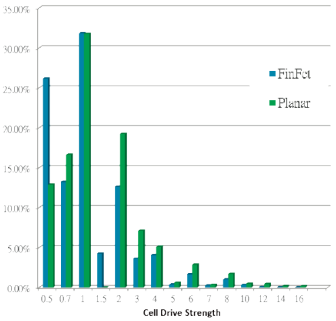


$$\text{3D Factor}: \frac{W_{EFF_FINFET}}{W_{BULK}} = \frac{2 \cdot H_{FIN} + T_{FIN}}{F_{PITCH}}$$

FinFET

Power and Device Tuning Challenges

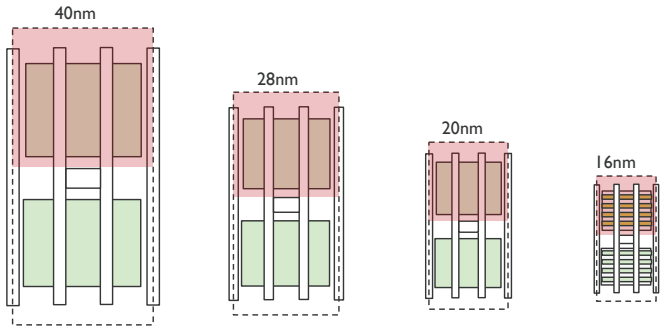
Drive Distribution FinFET versus Planar



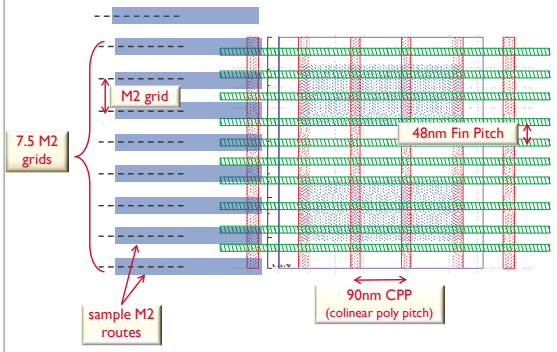
- Power Tuning
 - Dynamic power is tracking VDD scaling; little or no benefit from device capacitance scaling
 - Difficult to reduce power for "slow" design
 - Limited choice for power-gated header/footer devices
 - Lack of body effect in FinFET
- Device Tuning
 - True balanced beta ratios are not generally possible
 - Significant focus on low-power cells
 - Benchmarking shows a significant reduction in the average drive strength usage in FinFET versus planar

Standard Cell Transistor Widths

Now discrete due to fins



Standard Cells and Metal / Fin Gear Ratio



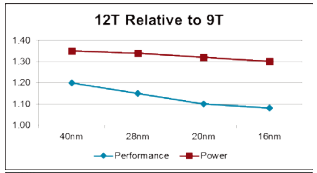
- M2 pitch does not equal fin pitch
- Must consider required fin and M2 pitch
 - Yields a limited number of cell heights
 - Need interger number of fins
- Designer wants 3 active p and n fins
 - Need 2 'dummy' fins between active areas
 - Need 1 'dummy' fin at top and bottom boundary
- 3p + 3n + 2 dummy + 2 boundary = 10 fins
- 10 fins * 48nm fin pitch = 480nm cell height
- 480nm height / 64nm M2 grid = 7.5 tracks

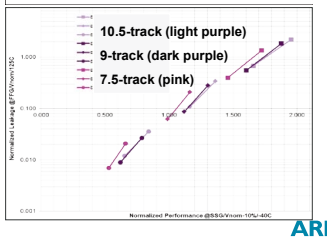
Fin illustrations may have minor misalignments



Trends for Standard Cell Libraries

- FinFET processes provide
 - Major push in performance, or
 - Major reduction in power for same performance
- Performance uplift enables higher density libraries compared to bulk
 - 12-track libraries are not desirable, being replaced with 10.5-track high-performance libraries
 - 9-track high-density libraries still very useful
 - 7.5-track ultra-high density libraries enable area scaling

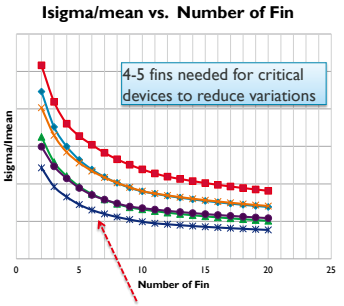




FinFET-based SRAM

- Pros:
 - Better current at same Vdd
 - Low variability (as compared to planar)
 - Lower leakage
- Cons:
 - Transistor width is a quantized number
 - Read disturb, write tradeoff becomes challenging

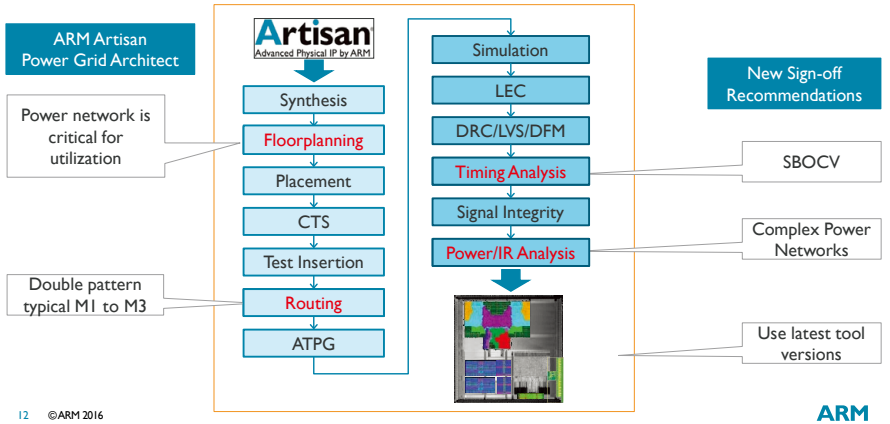
FinFET SRAM Bit Cell	PU	PG	PD	Comments
Cell 1: No. of Fins	1	1	1	High Variation; possible READ and Write Margin concern
Cell 2: No. of Fins	1	2	2	
Cell 3: No. of Fins	1	3	3	PU variation may lead to READ Margin issue



Variation goes up with less Fin

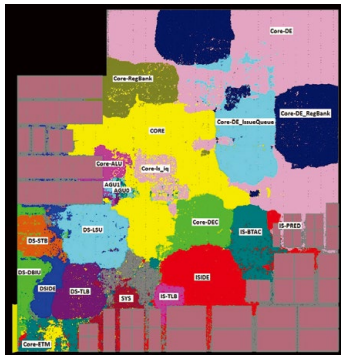
Implementation experiments details for Cortex-A73

Advanced EDA Flows and FinFET Effects

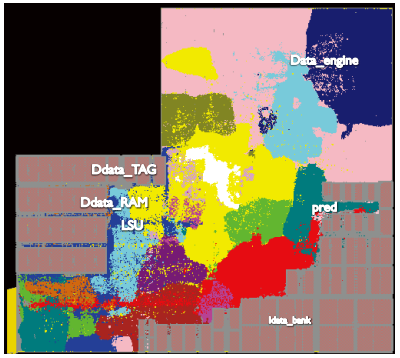


Floorplan exploration: Cortex-A73

A73 floorplan using 28HPC+



A73 floorplan using 16FFC

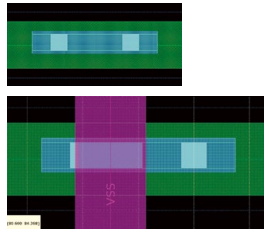


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FinFET Challenges for Power Grid Design

- Double pattern M1, M2 and M3
- Half-track libraries
 - Different rails for VDD and VSS
 - Sometimes V1 needs to be inserted post-route
- Pitch misalignment
- Complex DRCs
- Row end, top/bottom, and corner cap boundary cells are required

Default usage of PnR tool power grid commands will not create correct grids



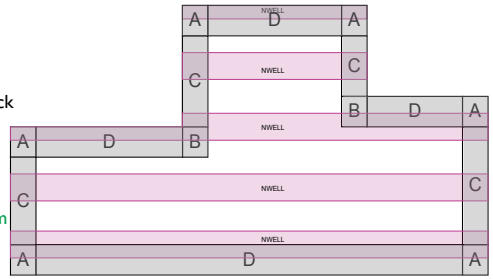
- Alternate power rails are supported to optimize network based on design power density
- Upper picture: M2 totem example
- Lower picture: M2 totem with M3 or M5 strap

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Special Library Cells – Boundary Finishing Cells

- Boundary finishing cells included to support design rules for block edges
- A = CNRCAP
 - Placed in outer corners of a block
- B = INCNRCAP
 - Placed at inside corners of an L-shaped block
- C = ENDCAP
 - Placed at the ends of rows
- D = TBCAP
 - Placed above and below the top and bottom rows of a block

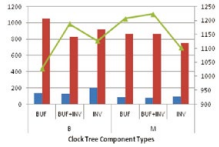
- Placement options:
 - By designer using code snipets in user guide
 - By ARM Power Grid Architect

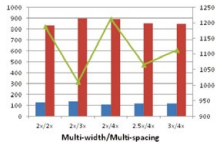


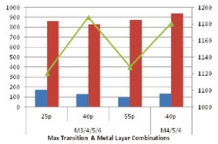
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POP IP – Clock Tree Synthesis

- Choosing the optimal clock-tree components – BUF vs INV, driving strength
 - Use INV cells, not BUF cells
 - Use the lowest V_T and shortest channel length available
- Clock nets NDR guideline – width and spacing
- Guidelines for routing layers, shielding, max. transition
- Recommendation for buffer drive strength, VT selection and channel length
- CTS based on MCMM analysis







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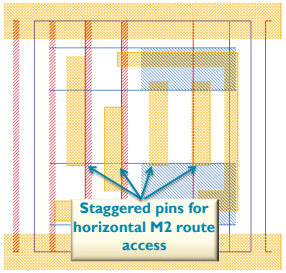
Routing Guidelines

DO

- Use the placement and routing options contained within ARMTech
 - TCL files for ICC and EDI
- Use the latest versions of the tools in most cases
- Carefully design power grid for optimal routing
- Complete placement of design including FILLer cells before routing

DO NOT

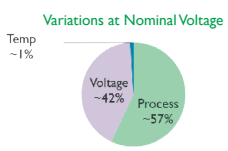
- Do not route on M1
 - M1 outside of pin shapes can cause unfixable double-pattern violations
- Do not route using wrong-way routing on double pattern layers (M2/M3)
 - Ok for router to use small wrong-way jogs

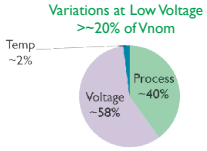


16FF Signoff Overview

ARM recommendations are consistent with TSMC recommendations

- Control over-margining; address variation
 - Signoff with SBOCV derates
 - No more using a single OCV value for a design
- SBOCV* accounts for local variation
 - Per cell derate values
 - Based on path depth and PVT corner
 - Variation decreases as path increases
 - Variation increases as voltage decreases





- Standard Signoff Corners
 - Setup+Hold: hot+cold SSGNP+SBOCV*
 - Hold only: hot+cold FFGNP+SBOCV*
- Stage-based OCV (SBOCV) Tables
 - Derate tables go in a side file
 - Four tables for each cell: early, late, rise, fall
- Stastical Hold Constraint Margin (SHCM)
 - Includes local variation margin in hold and recovery constraint tables in the Liberty model

**SBOCV requires using SHCM or additional margin for hold*

PPA detail for Cortex-A73

- This slide will show PPA achieved with various experiments and implementation run using ARM core Cortex-A73 with 28HPC+ and 16FFC processes.
- Due to confidential reasons, it can not be printed in handbook

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